Advanced Triggering with the TLA700 Series Logic Analyzers

Today's digital designers need a complete analog/digital debug tool kit that includes both advanced logic analyzer and digitizing storage oscilloscope (DSO) triggering capabilities.

Whether troubleshooting digital circuits for timing problems or analyzing digital prototypes for device characterization, examining today's high-speed signals can be a daunting task. As clock speeds continue to rise, fast edge rates and long board traces can work together to produce transmission line effects such as undershoot, overshoot, crosstalk, ringing on nodes, and other anomalies that can adversely affect the proper functioning of digital circuits. It's imperative, therefore, that designers not only have the ability to analyze the digital characteristics of their circuits, but the analog characteristics as well. To accurately characterize digital devices and troubleshoot timing problems when they occur, designers also need the ability to trigger on both complex digital events and analog signal anomalies. And they need to observe the details of their signals in both digital and analog domains.

In other words, today's digital designers need a complete analog/digital debug tool kit that includes both advanced logic analyzer and digitizing storage oscilloscope (DSO) triggering capabilities. In the logic analyzer realm, the tool kit should include a fast, versatile triggering mechanism capable of triggering on critical timing problems such as setup-and-hold time violations or glitches. In the DSO realm, the triggering capabilities should include edge, slew rate, glitch, pulse width, timeout, runt pulse, logic, and setup-and-hold triggering. Sophisticated design engineers will also find useful the ability to trigger the logic analyzer from the DSO and vice-versa.

In this technical brief, we'll briefly review the traditional digital circuit analysis paradigm and why it's ineffective for today's faster circuits. We'll discuss a new paradigm for circuit analysis, developed by Tektronix, that specifically addresses the shortcomings of the old testing methods. And we'll review what triggering is and why it's important.

Then, we'll discuss advanced logic analyzer triggering under the new paradigm (see Section 1), focusing on the advantages of using a Trigger State Machine rather than traditional Level Triggering. A typical application of setup-and-hold triggering will illustrate these advantages.

We'll examine the benefits of advanced DSO triggering (Section 2) and explain the advanced triggering modes now available. An application of pulse-width triggering will illustrate these benefits.

Finally, we'll discuss intermodule triggering (Section 3), perhaps the most powerful and useful feature of the new circuit analysis paradigm, which allows users to trigger a logic analyzer module from a DSO module and vice versa. It will include explanations of simple intermodule triggering, intermodule trigger arming, intermodule signal usage, and intermodule signal timing considerations.

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Enabling Innovation

The Traditional Circuit Analysis Paradigm

In the traditional circuit measurement and analysis paradigm, digital circuit designers typically employ multi-channel general purpose logic analyzers for digital or state analysis and either specialized high-speed logic analyzer modules or oscilloscopes for timing analysis. The conventional general purpose logic analyzer is simply too slow for timing analysis – it can't capture the fast rising and falling edges of today's high-speed signals across dozens of channels.

To get the extra speed needed for timing analysis, equipment manufacturers sacrifice channel count in specialized logic analyzer modules or oscilloscopes. In the traditional approach, if you want more acquisition speed, you have to reduce the number of channels that can be acquired simultaneously. Those willing to trade channels for speed quickly find that they've compromised their triggering capabilities as well.

A New Paradigm for Digital Circuit Analysis

The Tektronix TLA700 Series is built upon a modular platform that redefines the tools used for digital design analysis. This innovative design allows the TLA700 Series to be equipped with both logic analyzer and DSO modules and ensures that acquisitions made by logic analyzer modules are automatically time-correlated with acquisitions made by DSO modules.

In addition, the TLA700 Series implements a breakthrough technology called MagniVu™ – a super-fast digital sampler that enables each logic analyzer module to deliver 500 picosecond (ps) timing resolution on all of its 136 channels. This capability not only makes troubleshooting easier but, more importantly, it opens up an area of measurement capability previously unattainable with traditional logic analyzers – comprehensive timing verification. With MagniVu technology, the TLA 700 Series produces enough detailed timing information to support in-depth timing verification simultaneously with state analysis on each and every channel without having to re-probe or use an oscilloscope or expensive, specialized timing modules.

At the same time, the TLA700 Series provides the advanced triggering capabilities digital designers need to isolate timing anomalies. These advanced triggering capabilities fall into three categories – logic analyzer triggering, DSO triggering, and intermodule triggering. With intermodule triggering, designers are able to trigger one module from an event captured by another.

What Is Triggering and Why's It Important?

Triggering is an important concept for logic analyzers and DSOs because both are acquisition instruments built with circular memory buffers. A circular buffer basically stores data continuously, storing each new sample in the next available location in memory. When the buffer is full, it simply wraps around and stores each subsequent sample over the "oldest" sample in memory (the one that's been stored longest). The primary responsibility of the trigger mechanism is to stop the acquisition at the right time so that the sampled information left in memory represents the "slice-in-time" the user needs to view. The trigger mechanism can also be used to count or time events or to control the selective storage of data in real time.

In embedded microprocessor software debug applications, the system often doesn't really show signs of problems until long after they originate. The real challenge in triggering a logic analyzer in these applications is in recognizing very complex events that characterize the symptom (externally visible evidence of the problem). Since the root cause of problems actually precede the visible symptoms by long periods of time, designers use sophisticated triggering mechanisms to capture data leading up to the symptom. They then rely on deep acquisition memories to allow them to look backwards far enough in time to find the actual cause.

In hardware debug applications, the cause and the symptom are generally in closer chronological proximity to one another. Also, since effective timing analysis requires a much faster sample rate than embedded microprocessor software applications, the window of time encompassed by the entire acquisition is generally much shorter. For these reasons, hardware debug applications often require the user to trigger on the cause, rather than the symptom.

Section 1: Advanced Logic Analyzer Triggering

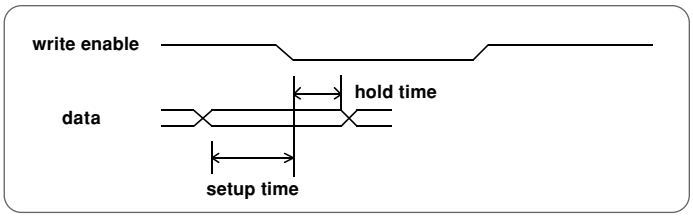
With 500 ps resolution across all 136 channels of the logic analyzer modules, finding subtle timing problems such as glitches, delays, and noise becomes a straightforward process. Coupled with advanced triggering capabilities, designers can use this high-resolution logic analyzer to isolate the root causes of timing problems in detail across all channels when they occur. It's especially useful for isolating troublesome anomalies that occur infrequently – such as those caused by marginal timing or crosstalk that's affected by data patterns or frequency.

If a processor reads a value that's invalid, for example, and causes a system to fail, the TLA700's logic analyzer module can be used to trigger on the faulty read cycle. The designer can then use the high-speed MagniVu memory to see the detailed timing of every signal around the critical event that triggered the acquisition.

State Machine Triggering vs. Level Triggering

Most logic analyzers allow the user to specify a list of events that can be sequentially evaluated, usually culminating in the triggering of the analyzer. Most allow some degree of conditional tests at each level of the sequence, with some ability to loop back to other levels or to reset the sequence if a particular condition fails. These conditional tests are generally referred to as levels or states. Regardless of the terminology employed, most implement these as sequential conditions with fixed logic choices that allow a very limited set of actions.

The TLA700 Series uses sophisticated trigger circuitry called a trigger state machine. While any logic analyzer trigger mechanism is technically a state machine of one form or another, the difference is that the TLA700 Series trigger state machine is implemented as a true random-access, fully programmable state machine rather than one with "hardwired" or fixed sequential logic. This means the TLA700 Series can evaluate several "If-Then-Else" conditions simultaneously; other analyzers can only evaluate such conditions one-at-a-time. It can evaluate much more complex combinations of events and execute more extensive combinations of actions. It allows the user to draw a state diagram of the circuit behavior and enter that diagram directly into the trigger program.



▶ ***Figure 1.*** *Timing diagram of setup-and-hold triggering*

Trigger State Machine Characteristics

The TLA700 Series trigger state machine can accommodate up to sixteen states, with each state consisting of one to four expressions called "If-Then-Else" clauses. Each "If-Then-Else" clause can evaluate a combination of up to eight events and can specify up to eight actions.

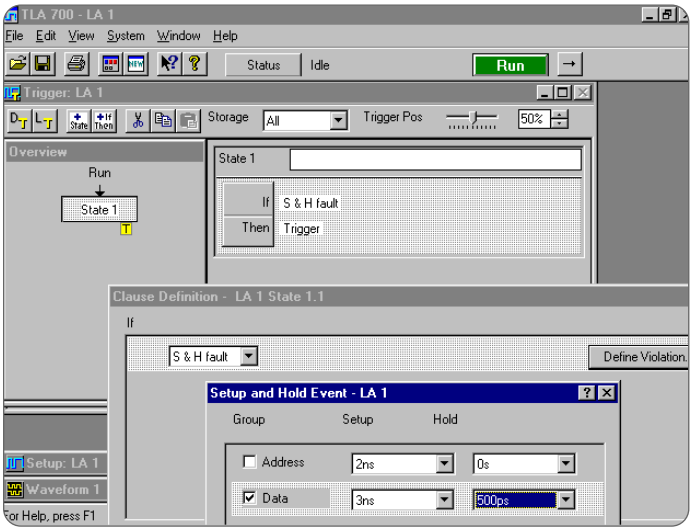
On a given clock sample, all If-Then-Else clauses in the current state are evaluated simultaneously. The first clause in the list whose expression of conditions is found true prevails and all actions associated with it are executed. If no clause prevails, the trigger state machine remains in the current state and no actions are initiated.

The TLA700 Series allows the user to evaluate events with: channel or group Event Recognizers (see description below), Glitch Recognizers, Setup-and-Hold Recognizers, Counter values (there are two 51-bit, 250 MHz counters), Signals from other modules or the external signal input to the mainframe, or Anything (always evaluates TRUE).

The user may also execute the following "actions:" Trigger Module, Trigger System, Go To (another state), Increment/Reset Counter, Start/Clear/Stop Timer, Set/Clear Signal (from other modules or the external signal input to the mainframe), Arm (another) Module, Store/Don't Store Sample, or Do Nothing (useful in some logical combinations).

Event Recognizers

Any individual channel or group of channels can be evaluated to test if its logic value changes or matches any logic value, masked bit pattern, or range of values. Logical combinations of these tests can produce very useful hybrid events such as counting the number of times a group's value changes to match a specific value but not counting subsequent samples that continue to match that value. Logical values for comparison can be entered in a wide variety of numeric radices: hexadecimal, binary, signed decimal, unsigned decimal, octal, or symbolic.



▶ ***Figure 2:*** *This screen shows the logic analyzer setup for triggering on a data access that exhibits a violation of setup-and-hold time. If the value of the data bus changes less than 3 ns prior to or less than 500 ps after the active clock edge, the logic analyzer will trigger.*

Glitch Triggering

The TLA700 also includes a built-in glitch detector that can continuously hunt for glitches on every channel. The glitch detector continuously monitors the data stream from the sampler. When a glitch occurs, the detector triggers the analyzer and highlights the glitch on screen. The designer can then use MagniVu technology to actually see the number, width, and placement of glitches within the sample period with 500 ps resolution, or view the glitch with the DSO to determine why it happened.

Glitch detection is especially useful when analyzing clock performance. In high-speed logic design, clock distribution and signal quality are foremost concerns. With the TLA700 Series, clock signals can be acquired at each critical distribution point, allowing designers to see the effects of clock distribution implementation. The glitch detector is used to help track down glitches in the clock lines.

Setup-and-Hold Triggering

The TLA700 Series can also directly trigger on violations of the most crucial synchronous timing parameters – setup-and-hold time. The built-in setup and hold checker detects transitions in the input signals after they are acquired with the TLA700's high-speed oversampler. The transitions are then skew-adjusted and violations are flagged if the transitions are within the interval defined by the user. With this capability, the designer can, for example, exhaustively examine the performance of a system's entire data bus. Even the margins for setup-and-hold can be characterized. This capability allows designers to determine how well the circuitry will accommodate component and temperature variations. In addition, timing of the data bus relative to all the different memory and attached peripheral devices can be verified.

Other Triggering Resources

Another versatile triggering resource available to the TLA700 Logic Analyzer module is the counter/timers. A counter can be used to trigger the logic analyzer module on a specific number of transition events, on a specified number of times data is written to a specific I/O device, how many times a subroutine was called, or any number of other possibilities.

A timer can be used to precisely measure the duration of specific events. A designer may want to know, for example, how long it takes for an interrupt to be handled by a processor. When characterizing a device or system, a designer may simply want to know whether a specific event is happening or not.

A Typical Application: Verifying SRAM Setup-and-Hold Design Margins

As stated above, the TLA700's advanced triggering capabilities, coupled with its high-speed MagniVu memory, makes possible not only more accurate troubleshooting, but also a measurement capability previously unattainable with traditional logic analyzers – comprehensive timing verification. The TLA700 Series produces enough detailed timing information to support in-depth analysis and verification of timing margins.

For example, Figure 1 shows the address setup-and-hold times for data write cycle. If the setup time design goal has been defined to be 3 ns, the user can easily instruct the logic analyzer module to trigger on any interval less than 3 ns. (see Figure 2). The Windows™ 95-based user interface makes setting up the setup-and-hold times a simple matter of filling in the blanks.

To determine the actual setup-and-hold time margins, the designer can enter larger and larger time intervals until the system fails. With this capability, the designer can locate potential problem areas in the first prototype instead of more costly second, third, or even final versions.

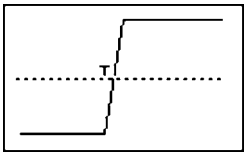
It should be noted that setup-and-hold triggering only applies when using the TLA700's synchronous acquisition mode, using the clock supplied by the system under test (external or custom clock). In the asynchronous mode, the clock is generated internal to the logic analyzer (internal clock), and exists only inside the analyzer. The timing of the user's data is inherently asynchronous to that clock, therefore the concept of setup-and-hold triggering does not apply in this mode.

Section 2: Advanced Triggering with DSO Modules

With a 5 GS/s sample rate and a bandwidth of 1 GHz at the probe tip, the TLA700 DSO modules can help designers pinpoint the root causes of timing problems.

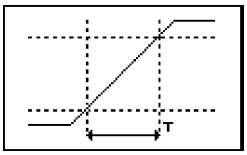
DSO Triggering Modes

Edge Triggering is the primary triggering mode used by traditional oscilloscopes and is useful for aligning the transitions of a particular input signal with the trigger point.



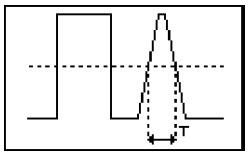
The user specifies a voltage level and either a rising or falling edge of the desired channel. The DSO triggers when the input signal crosses that voltage level in that direction.

Slew-Rate Triggering goes beyond edge triggering by adding the element of time. It enables the user to selectively trigger on edges that are too fast or too slow. Signal edge rates are often reduced by the influence of elements in the signal path that are not on the schematics. Slow transitions can reduce timing margins and increase a circuit's susceptibility to a variety of signal quality problems. Signals with slew rates faster than expected (or needed) can radiate troublesome energy at high frequencies.



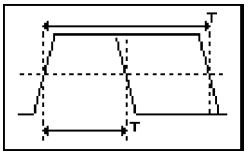
With slew-rate triggering, the user may specify two voltage levels, rising or falling edge of the desired channel, a time value and whether the actual slew rate should be faster or slower than the time specified. The DSO triggers when the input signal crosses the designated voltage levels in the designated direction, but only if the slew rate of the signal fails to meet the specified time limit.

Glitch Triggering allows the user to trigger on even the fastest digital pulses when they are shorter or longer than a precise time limit. This capability enables the user to see the causes of glitches and examine their effects on other signals, even when the glitches occur infrequently. It's especially useful if the glitches are so short they violate a minimum pulse width specification or if they occur on a signal when it shouldn't be moving.



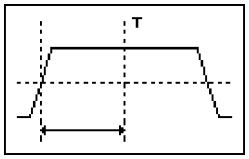
To initiate glitch triggering, the user specifies a threshold voltage level, the expected polarity of the glitch to be captured, the desired channel to evaluate, a time value, and whether the glitch (or other pulse) should be faster or slower than the time specified. The DSO module will trigger when the input signal exhibits a pulse relative to the designated threshold voltage and with the specified polarity, but only if the duration of the pulse fails to meet the specified time limit.

Pulse Width Triggering is similar to glitch triggering, but adds the versatility of allowing the user to specify a range of acceptable time values. This capability is very useful for examining circuits that generate pulses whose duration needs to be consistent or tightly controlled. Using this trigger mode, the user can watch a signal indefinitely and trigger on the first occurrence of a pulse whose duration is outside the allowable limits. The user can also run repeated tests, varying the limits each time, to characterize a signal's behavior and determine how much timing margin is available.



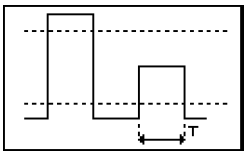
To initiate pulse width triggering, the user specifies both a maximum and minimum acceptable pulse duration, a threshold voltage level, the desired pulse polarity, which channel to evaluate, and whether the pulse should be inside or outside the specified time limits. The DSO triggers when the input signal exhibits a pulse relative to that threshold voltage and with the specified polarity, but only if the duration of the pulse fails to meet the specified range of time limits.

Timeout Triggering is especially useful for triggering on signals that hang in an active state when they fail. Other time-qualified trigger modes, by definition, are unable to complete a time measurement until the event (glitch, pulse width, etc.) terminates. The user can employ these other modes to trigger on pulses that exceed a time limit. However, since the pulse measurement is not actually evaluated until the trailing edge of the pulse occurs, signals that go active and never return to their inactive state will not generate a trigger, even though the specified time has elapsed. Timeout triggering eliminates this problem by triggering when the specified time has lapsed, without waiting for the pulse to end.



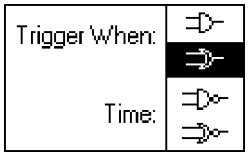
The user initiates timeout triggering by specifying a maximum acceptable pulse duration, a threshold voltage level, the desired pulse polarity, and the channel to evaluate. The DSO triggers when the input signal stays active for the specified period of time regardless of whether it returns to the inactive state.

Runt Pulse Triggering allows the user to capture and examine pulses that cross one logic threshold but not both. This capability can reveal potential signal quality problems that are difficult to pinpoint with a logic analyzer alone. It allows the user to run repeated tests, varying the threshold voltages each time, to characterize a signal and determine how much noise margin is available in the design. It's especially useful for characterizing and troubleshooting problems with clock distribution in microprocessor-based or other synchronous designs.



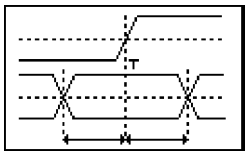
To initiate runt pulse triggering, the user specifies threshold voltage levels for both high and low states of the logic family being used, the desired runt pulse polarity, a time value, and whether the pulse should be longer than the time specified. The DSO module triggers when the input signal exhibits a pulse of the specified polarity that crosses the first threshold voltage but goes back across that threshold without ever reaching the second. The user can choose to trigger on any such runt pulse or only if the duration of the pulse exceeds the time specified.

Logic Triggering is an extremely flexible triggering mode that allows the user to trigger on any logical combination of input channels. Logic triggering has endless application in verifying the operation of digital logic. With time qualification, it's especially useful for finding race conditions and avoiding potential timing problems in critical logic paths.



To initiate logic triggering, the user specifies the threshold voltage and polarity of all the input signals used (limited to the number of channels on a single module). Any inputs that are not desired in the logic comparison are easily disabled by specifying an "X" (meaning "don't care," such as when specifying a logic analyzer trigger) for that channel. The user also specifies a logic function – AND, OR, NAND, or NOR – a time value, and whether to trigger any time the combination occurs, or only if its duration is longer or shorter than the time specified. The DSO triggers when all input signals exhibit the specified logic pattern for the specified time period.

Setup-and-Hold Triggering makes it easy to capture specific details of both signal quality and timing when a synchronous data signal fails to meet setup-and-hold design specifications. Any DSO can acquire and display the timing relationship between a random transition of clock and data by triggering on the clock edge. Some use eye-diagrams to show a distribution of many transitions. But only setup-and-hold triggering ensures that you can deterministically trap a single transgression of setup-and-hold time that would almost certainly be missed by the other methods.



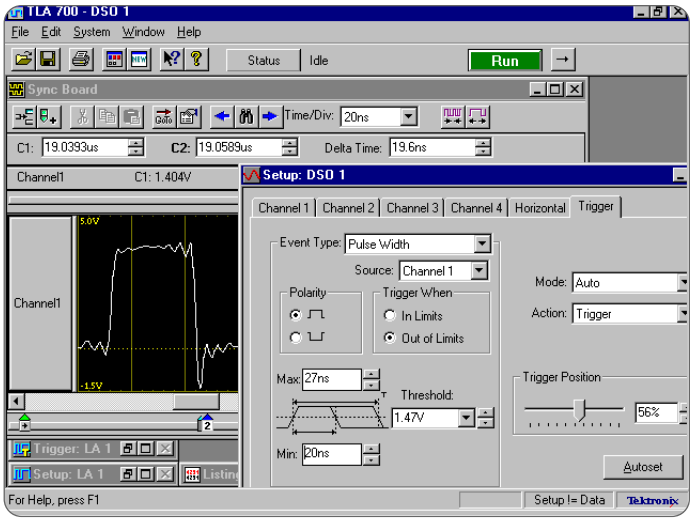
To initiate setup-and-hold triggering in the DSO module, the user selects one channel for the clock input and one for the data input; then specifies a clock edge, a threshold voltage level for each input, and limit values for both setup time and hold time. The DSO triggers when the data input signal crosses its threshold within the specified setup-and-hold time limits relative to the selected edge of the clock input.

An Application of Pulse Width Triggering

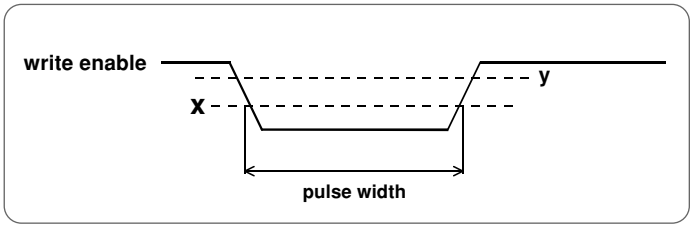
Returning to the previous SRAM example, the TLA700's DSO module can be used to trigger on the minimum pulse width spec of the write enable. If the pulse width spec is 20 ns, for example, the DSO can be instructed to trigger on pulse widths less than 20 ns. This screen shows the DSO setup for triggering on a pulse that is either shorter than 20 ns or longer than 29 ns at a threshold of 1.47 Volts. The acquired pulse is shown in the waveform display in Figure 3.

This capability can help the designer isolate, for example, transmission line effects that may cause ringing on a line; which, in turn, may cause the pulse width to seem shorter than specified because an overshoot or undershoot caused the write enable signal to cross the threshold.

The designer can also use this capability to determine how much the actual pulse width changes when the threshold is moved from level x to level y, as shown in Figure 4.



▶ ***Figure 3.*** *This screen shows the DSO setup for triggering on a pulse that is either shorter than 20 ns or longer than 29 ns at a threshold of 1.47 Volts. The acquired pulse is shown in the waveform display on the left*



▶ ***Figure 4.*** *Timing diagram of pulse width triggering with DSO module.*

Section 3: Intermodule Triggering

Perhaps the most powerful and useful feature of the TLA700 is its ability to provide intermodule triggering, with complete time-correlation between modules. In other words, the logic analyzer modules can be used to trigger the DSO modules, and vice versa, and all acquisitions will be automatically time-correlated. No matter how the designer approaches a problem, whether through the analog domain or the digital, the TLA700 will help the designer get to the root of the problem quicker and easier.

Simple Intermodule Triggering – The simplest form of intermodule triggering is so easy to use the user may not necessarily think of it as intermodule triggering. It's when trigger resources are used as described in either the logic analyzer triggering or DSO triggering sections to generate a System Trigger instead of a Module Trigger. All this requires is that the user change the action of the trigger mechanism used. Then, when the specified module satisfies its specified trigger conditions, all modules will trigger and display their data. All data from all modules is automatically time-correlated.

To ensure consistent results when triggering both modules from one module, one of the modules should be set up to NOT trigger on its own.

The DSO module has a trigger event type selection called "Wait for System Trigger." If the user is triggering both modules from the logic analyzer, this trigger event type should be selected along with trigger mode "Normal," not "Auto." The "Auto" trigger mode is the conventional analog oscilloscope trigger mode that forces a trigger after a fixed period of time (about 500 ms). It will override the "Wait for System Trigger" event if selected and, in this case, would produce confusing results if the Auto-trigger timer terminated before the other module happens to trigger.

If the user is triggering both modules from the DSO, the logic analyzer module can easily be setup to NOT trigger itself by using the "Default Trigger" command or toolbar button to restore the default trigger setup. The user should then go into the "If-Then-Else" clause and change the action from "Trigger" to "Do Nothing."

Intermodule Trigger Arming – The next level of intermodule triggering involves setting up individual trigger programs in the logic analyzer and DSO modules, but using the trigger mechanism of one to "Arm" the trigger mechanism of the other when certain events are observed in the first. Once a module receives an "Arm" signal from another module, it latches that signal and remains armed until the acquisition is complete.

For example, the user may suspect that signal quality is the potential cause of a serious problem that only shows up when certain sections of the hardware are active. Perhaps the user has checked signal quality with the DSO but is not sure that it's acquiring at the right time. The logic analyzer trigger state machine can be used to detect when the hardware is active and Arm the DSO to trigger on the next occurrence of a runt pulse that reflects the problem. Once the DSO observes the desired condition, it can trigger both modules in order to view both the signal quality as acquired by the DSO along side the details of signal behavior it caused as acquired by the logic analyzer.

Again, the user should verify that the selected trigger mode of the DSO module is "Normal," not "Auto." The "Auto" trigger timer will override the "Armed by LA 1" qualification in this case and produce confusing results.

Intermodule Signal Usage – The most advanced level of intermodule triggering involves setting up individual trigger programs in the logic analyzer and DSO modules and using the trigger mechanism of each to dynamically pass signals to the trigger mechanisms of others. The mainframe can be configured through the user-interface to logically combine (AND/OR) the outputs of multiple modules that drive each signal. These capabilities can be used to identify complex events involving multiple modules.

External Signals – Configurable signals are also available external to the mainframe. These signals are available on BNC connectors on the TLA704 or on SMB connectors on the front panel of the TLA711 controller module. The TLA711 includes a P6041 probe that can be used to bring one of these signals to a BNC connector.

The External Signal Output is a TTL-compatible output, back terminated into 50 ohms. The user-interface allows the user to configure the mainframe so that any of the four intermodule signals drive this output.

The External Signal Input is a TTL-compatible, level sensitive input that can be configured via the user-interface to drive any of the mainframe intermodule signals.

Also provided are an external trigger output, which is asserted whenever a system trigger occurs, and an input, which will generate an immediate system trigger.

Intermodule Signal Timing Considerations

When using intermodule triggering, it's important to understand the timing behavior of signals between modules and the nature of different module types.

The effective intermodule System Trigger delay is the effective time difference at the probe tips from the occurrence of an event that one module observes and uses to generate a system trigger until the occurrence of data that is seen by the second module at the time the System Trigger signal has arrived and has triggered that module. The effective System Trigger delay from a logic analyzer module to a DSO module is about 360 ns. From logic analyzer to logic analyzer, it's approximately 70 ns. From DSO to DSO, it's about 50 ns. And from DSO to logic analyzer it's about –240 ns.

The effective intermodule Arm delay is the effective time difference at the probe tips from the occurrence of an event that one module observes and uses to generate an arming signal until the occurrence of data that is available for triggering on the second module once the intermodule Arm signal has arrived and has armed its trigger machine. The effective Arm delay from a logic analyzer module to a DSO is approximately 360 ns. From logic analyzer to logic analyzer it's about 110 ns1. From DSO to DSO it's about 60 ns. And from a DSO module to a logic analyzer module it's about –190 ns.

The effective intermodule Signal delay is the effective time difference at the probe tips from the occurrence of an event that one module observes and uses to generate a signal until the occurrence of data that is available for triggering on the second module once the inter-module signal has arrived and can be tested in its trigger machine. The effective intermodule Signal delay from one logic analyzer module to another is about 120 ns[1]. From a DSO module to a logic analyzer module it's approximately –180 ns. There are no intermodule signals from a logic analyzer module to a DSO module, or from a DSO to a DSO. This is because the DSO trigger mechanism doesn't use signals other than to Arm it or to generate a System Trigger.

Notice that the delay times for signaling from a DSO module to a logic analyzer module are negative. This is because the internal data pipeline delays for a logic analyzer are much longer than for a DSO. And that means that even though the DSO has to satisfy its trigger condition first, it actually does so and gets its signal to the logic analyzer before the data it triggered on has propagated all the way into the logic analyzer machine. This causes no serious problems, but can be confusing if not understood correctly.

Because of this timing delay, even the simple case of using the DSO to trigger all modules causes some interesting results. Each module always records its own trigger in its own acquisition. The System Trigger is associated, if possible, with the module that actually caused it. The data display shows a trigger "T" for the logic analyzer module before the trigger "T" for the DSO module and before the System Trigger "T". This is because the point at which the logic analyzer triggered relative to the data it was acquiring is effectively earlier than the point at which the DSO triggered relative to the data it acquired. The System Trigger is correctly associated with the DSO module, even though the effective logic analyzer trigger point appears first.

1 All signals received by a logic analyzer module are actually recognized on the first valid sample after the specified delay. (The additional time delay incurred waiting for the next valid clock varies with the clocking setup and the timing of external clocks.)

Conclusion

Quickly tracking down the cause of timing and signal quality problems in today's high-speed digital hardware requires logic analyzers and DSOs with sophisticated triggering capabilities. The TLA700 Series offers advanced triggering in both analog and digital domains that dramatically streamlines the entire process of system verification and characterization for the designer. The versatile Trigger State Machine of the TLA700 Series logic analyzers, with its arsenal of resources, enables digital designers and engineers to capture virtually any digital event. The wide variety of time-qualified fault-trigging modes of the TLA700 Series DSOs ensures that even the most elusive analog event can't slip by. Advanced intermodule triggering makes it easy to trigger both logic analyzer and DSO modules from either an analog or digital anomaly. In addition, intermodule triggering enables all modules to "Arm" other modules so that they don't falsely trigger on something out of context. For sophisticated users, TLA700 Series modules can also pass intermodule signals, enabling them to trigger on tricky problems that dynamically cross both domains.

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